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speed-increasing circuit coupled between a first node and a second node, said first node being at an input terminal of the driver circuit and said second node being in a vicinity of an input terminal of one of the gate circuits coupled to an end of the first wiring.--

--17. The semiconductor integrated circuit device as claimed in claim 16, wherein the speed-increasing circuit includes a PMOS transistor.--

--18. The semiconductor integrated circuit device as claimed in claim 16, wherein the speed-increasing circuit includes an NMOS transistor and a buffer circuit is inserted at an input side of the second wiring.--

--19. The semiconductor integrated circuit device as claimed in claim 16, wherein the speed-increasing circuit includes a CMOS inverter having a PMOS transistor and an NMOS transistor.--

--20. The semiconductor integrated circuit device as claimed in claim 16, wherein a plurality of speed-increasing circuits are additionally inserted between an intermediate position of the second wiring and the vicinity of the input terminal of the gate circuit connected to a position corresponding to the intermediate position.--

--21. The semiconductor integrated circuit device as claimed in claim 16, wherein a plurality of buffer circuits are inserted at the input side of the second wiring.--

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--22. The semiconductor integrated circuit device as claimed in claim 16, wherein a buffer circuit is inserted at the input side of the second wiring.--

--23. The semiconductor integrated circuit device as claimed in claim 16, wherein the input signal is realized by a word line selecting signal; the driver circuit is realized by a word line driver; the first wiring is realized by a word line; and the gate circuits are realized by memory cells.--

--24. The semiconductor integrated circuit device as claimed in claim 16, wherein the input signal is realized by a clock input signal; the driver circuit is realized by a clock driver; and the gate circuits are realized by flip-flop circuits.--

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